THE ARMADEUS PROJECT

DATASHEET

APF9328 DEV LIGHT

8. November 2006
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<tr>
<th>Edition</th>
<th>Date</th>
<th>Changes</th>
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<tr>
<td>Edition 0.A (PCB ed 1)</td>
<td>16. February 2006</td>
<td>Initial version</td>
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<tr>
<td>Edition 0.B (PCB ed 1)</td>
<td>4. September 2006</td>
<td>Add signal tables</td>
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<tr>
<td>Edition 0.C (PCB ed 1)</td>
<td>8. September 2006</td>
<td>Fix error in signal tables concerning DAC_REF and DAC_OUT2. Rename DAC_OUT1 to DAC_OUTA and DAC_OUT2 to DAC_OUTB according to the DAC datasheet</td>
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<tr>
<td>Edition 0.D (PCB ed 1.1)</td>
<td>8. November 2006</td>
<td>Add APFDevLight photo</td>
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1.1 Introduction

The APF9328 Dev Light is low cost development board dedicated to the APF9328 single board computer.

This board offers access to the most used functionalities of the APF9328. It's price and prototyping zones makes it ideal for rapid development of simple applications.

Note: an APF9328 is mounted on the DevLight for this photo.

1.2 Mechanical Overview

Size: 100 mm x 75 mm (3.9” x 3”)

![APF9328 Dev Light](image-url)
1.3 APF9328 Dev Light Features

Input Power supply: 7 to 12V DC with resettable fuse
On board regulator: 3.3V / 1A max

Connectors:
- Ethernet (RJ45) with integrated isolation transformer
- USB slave (type B)
- DB9 header (RS232)
- Jack 2.5mm for power supply
- Two Hirose receptacles for APF9328

Reset: Tact switch
Boot: Jumper for selecting the boot mode

Prototyping zone: Two prototyping zone with 2.54mm pitch holes
Silkscreen: Allows to easily recognize the APF9328 pins

1.4 Handling precautions

Please ensure that should a board need to be returned to Armadeus, it is adequately packed, preferably in the original packing material.
Chapter 2: Hardware Description

The following section provides a detailed description of the functions available on the APF9328.
2.1 Connectors

2.1.1 RS232 (DB9)

This connector provides a standard RS232 interface without RTS and CTS signals. ESD and overvoltage protections are located on the APF9328.

Remark: a RS232 cable has to be used to connect the APF9328 DevLight to a PC

2.1.2 USB (Slave)

The USB slave connector allows connecting the APFDevLight to your PC. The board, if correctly configured, will be seen as a slave device.

The USB transceiver is located on the APF9328 board and no protection against ESD have to be foreseen as they are already provided by the transceiver.

2.1.3 Ethernet (RJ45)

If the APF9328 is equipped with the Ethernet controller (-E option) the Ethernet connector can be used to connect your APF9328 DevLight to your network.

2.1.4 Boot Jumper

If a jumper is mounted on this 2 pin connector, the APF9328 will start in bootstrap mode. This mode can be useful if the APF9328 bios (uBoot) has been corrupted or lost. The RS232 is used to transfer uBoot from your PC to the internal flash of the APF9328. For more information please see the APF9328 Software Guide.

Reminder! Do not forget to remove the jumper after uBoot recovery

2.2 Power Supply

A linear regulator provides supply voltage (+3.3V) required by the APF9328. You can use the output for your experiments but take care to not sink more current that the maximum allowed (see Features chapter)

This regulator accept an external voltage between 5 and 12V.

It has to be noted that the board input is protected against short circuits by means of a resettable fuse.
2.3 Prototyping Zones and Silkscreen

Two prototyping zones have been foreseen to quickly test your application without having to create a new PCB. The pitch between pads is 2.54mm.

You will see that between the two Hirose receptacles (connectors for the APF9328) several pads are provided. They are connected to the main functions of the APF9328 board (see table below for details). You can simply connect some wrapping wires between these pads and the ones of the two prototyping zones. For this purpose, the bottom side of the APF9328 DevLight provides a silkscreen allowing to quickly identify the function of each pads.

The table below described the placement of the signals (bottom view)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Signal</th>
<th>Signal</th>
<th>Signal</th>
<th>Signal</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSI_D2</td>
<td>CSI_D1</td>
<td>CSI_D0</td>
<td>LD3_B3</td>
<td>LD2_B2</td>
<td>LD1_B1</td>
</tr>
<tr>
<td>CSI_D5</td>
<td>CSI_D4</td>
<td>CSI_D3</td>
<td>LD7_G2</td>
<td>LD6_G1</td>
<td>LD5_G0</td>
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<tr>
<td>CSI_PIXCLK</td>
<td>CSI_PIXCLK</td>
<td>CSI_PIXCLK</td>
<td>LD11_R0</td>
<td>LD10_G5</td>
<td>LD9_G4</td>
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<tr>
<td>CSI_PIXCLK</td>
<td>CSI_PIXCLK</td>
<td>CSI_PIXCLK</td>
<td>LD15_R4</td>
<td>LD14_R3</td>
<td>LD13_R2</td>
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<tr>
<td>UART1_CTS</td>
<td>UART1_RTS</td>
<td>CONTRAST</td>
<td>REV</td>
<td>CLS</td>
<td>PS</td>
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<td>UART2_RTS</td>
<td>UART2_TX</td>
<td>UART2_RX</td>
<td>LSCLK</td>
<td>PLM_VSYNC</td>
<td>OE_ACD</td>
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<tr>
<td>UART2_CTS</td>
<td>UART2_CTS</td>
<td>SPI_RDY</td>
<td>SPI_SSN</td>
<td>SPI_SCLK</td>
<td>SPI_MOSI</td>
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<td>SSI0_TXFS</td>
<td>SSI0_TXCLK</td>
<td>SSI0_RXCLK</td>
<td>SSI0_RXDAT</td>
<td>SSI0_TXDAT</td>
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<tr>
<td>SSI1_RXFS</td>
<td>SSI1_TXFS</td>
<td>SSI1_TXCLK</td>
<td>SSI1_RXCLK</td>
<td>SSI1_RXDAT</td>
<td>SSI1_TXDAT</td>
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<tr>
<td>TOUT2</td>
<td>TIN</td>
<td>PWM0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L24N_3</td>
<td>L24P_3</td>
<td>L23N_3</td>
<td>L01N_5</td>
<td>L01P_5</td>
<td>L28P_5</td>
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<tr>
<td>L40P_2</td>
<td>L40N_3</td>
<td>L40P_3</td>
<td>L31P_5</td>
<td>L31N_5</td>
<td>L32P_5</td>
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<tr>
<td>L24N_2</td>
<td>L24P_2</td>
<td>L40N_2</td>
<td>L32N_4</td>
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<td>L22P_2</td>
<td>L23N_2</td>
<td>L23P_2</td>
<td>L20P_3</td>
<td>L20N_3</td>
<td>L21P_3</td>
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<tr>
<td>L21N_2</td>
<td>L21P_2</td>
<td>L22N_2</td>
<td>L22N_3</td>
<td>L22P_3</td>
<td>L23P_3</td>
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<td>L01P_2</td>
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<td>AIN7</td>
<td>AIN6</td>
<td>AIN5</td>
</tr>
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<td>L32N_0</td>
<td>L32P_0</td>
<td>L01N_2</td>
<td>AIN3</td>
<td>AIN2</td>
<td>AIN1</td>
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<tr>
<td>L31P_0</td>
<td>L31N_0</td>
<td>L32N_1</td>
<td>EOCN</td>
<td>REFP</td>
<td>DAC_REF</td>
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<td>L30P_0</td>
<td>L30N_0</td>
<td>L27P_0</td>
<td>L27N_0</td>
<td>L01P_0</td>
<td>L01N_0</td>
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<tr>
<td>L28N_1</td>
<td>L28P_1</td>
<td>IO1</td>
<td>L31P_1</td>
<td>L31N_1</td>
<td>L32P_1</td>
</tr>
<tr>
<td>L01P_1</td>
<td>L01N_1</td>
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<td></td>
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</table>
On the left prototyping zone (bottom view) the vias are free excepted the ones placed near the hirose connectors.

<table>
<thead>
<tr>
<th>TRSTN</th>
<th>TDO</th>
<th>TDI</th>
<th>TCK</th>
<th>TMS</th>
<th>CS5N</th>
<th>RWN</th>
<th>OEN</th>
<th>EB3N</th>
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On the right prototyping zone (bottom view) the vias are free excepted the ones placed near the hirose connectors (address labeled).

<table>
<thead>
<tr>
<th>A4</th>
<th>A3</th>
<th>A2</th>
<th>A1</th>
<th>A0</th>
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APF9328 Dev Light 0.D
### 2.3.1 APF9328 Features not accessible from the APF9328 DevLight

All the features of the APF9328 are accessible from the APF9328 DevLight excepted the following ones:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
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</thead>
<tbody>
<tr>
<td>24..32 / 88..97</td>
<td>A5..A23</td>
<td>Address Bus</td>
<td>28..35</td>
<td>D8..D15</td>
<td>Data Bus</td>
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<tr>
<td>36</td>
<td>CS1n</td>
<td>Chips Select 1</td>
<td>98</td>
<td>PA17</td>
<td>CS5n ready pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>118</td>
<td>EXTAL16M</td>
<td>External 16M clock input</td>
</tr>
<tr>
<td>23</td>
<td>EB2n</td>
<td>Enable for 16Bits write access</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>CS4n</td>
<td>Chips Select 3</td>
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